HPC@FER

Croatian HPC Competence Centre Day 2024

HPC ARCHITECTURE AND APPLICATION RESEARCH CENTER

UNIVERSITY OF ZAGREB
Faculty of Electrical Engineering and Computing

High Performance Computing at FER

- Projects
- Teaching

HPC

APPLICATIONS AND ARCHTECTURES

PARALLELISM

CONCURRENCY

HPC

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European Processor Initiative

epi

TÉCNICO LISBOA · EVIDEN · ETH zürich · Barcelona Supercomputing Center · KERNKONZEPT

SURF · JÜLICH Forschungszentrum · semidynamics · KALRAY · Fraunhofer

ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA · CHALMERS · FER · Faculty of Electrical Engineering and Computing · E4 COMPUTER ENGINEERING · CINECA · cea

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Research

High-performance computing (HPC) is one of the key enabling technologies having wider and longer-term effects on science and society. Forecasting climate evolution, space observation, preventing and managing large-scale natural disasters, developing, and understanding chemistry and physics of new materials, designing new personalized drugs, all require top HPC resources. Traditionally, HPC has given scientists deep insights into unexplored phenomena and systems of the highest complexity. However, HPC usage today is not confined to science only: industry, and even society at large is based on the ever-growing use of complex ICT solutions and resources. HPC, as one key element, can significantly reduce R&D costs and development cycles while producing higher quality products and services. Also, from a business perspective, investments in HPC provide high returns. Last, but not least, HPC is also crucial for national security and defense. It enables an increase of safety and security, by providing means to e.g. enable strong encryption technologies, simulate complex security threats, perform large-scale suspicious pattern detection in social networks.

Find out more in our sections about projects, Applications and Architecture.

European Processor Initiative

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Projects (Past, Present, and Future)

MEEP

www.meep-project.eu

DARE (to dream RISC-V HPC)

European Processor Initiative

Two pillars to make European ambition a reality

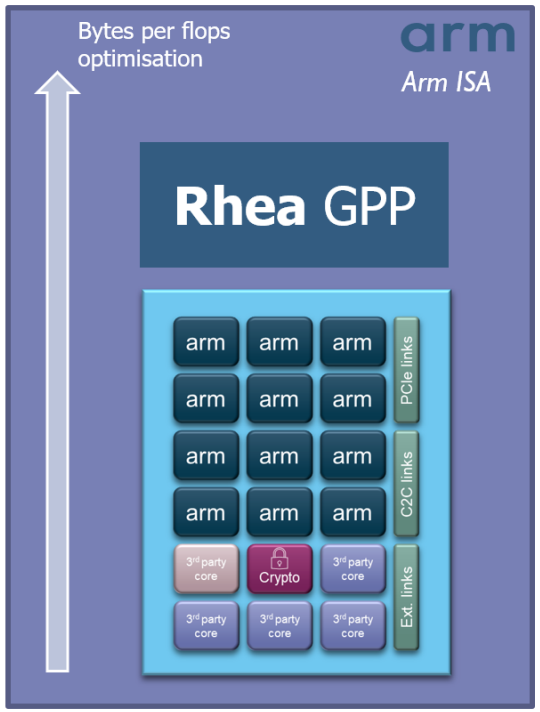
Empowering Europe's Semiconductor Future, uniting innovation and driving Progress

Leading the way in European Supercomputing, developing a World Class Supercomputing Ecosystem

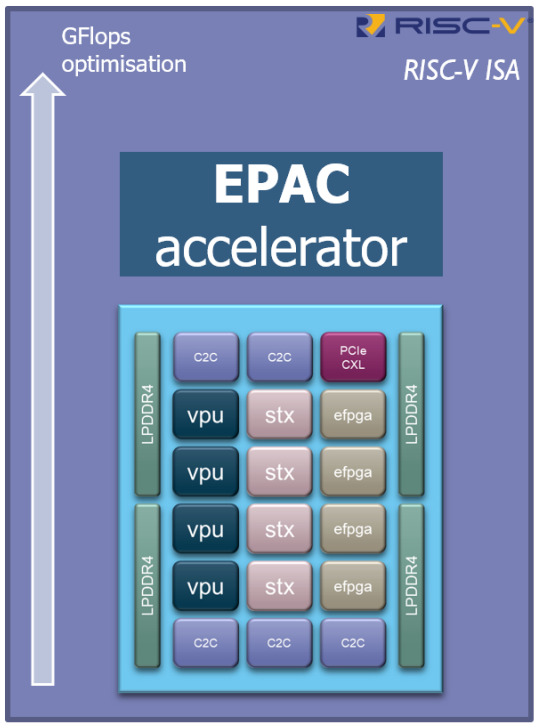
Projects: European Processor Initiative

EU chips fit for HPC usage – at Exascale level

General Purpose Processors:
Enable legacy & programmability

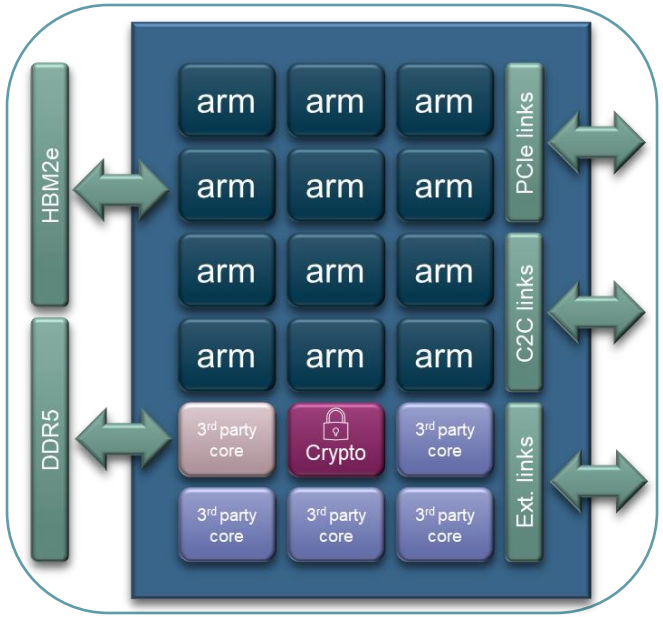


Accelerators:
Computing force



RHEA1: GENERAL PURPOSE PROCESSOR

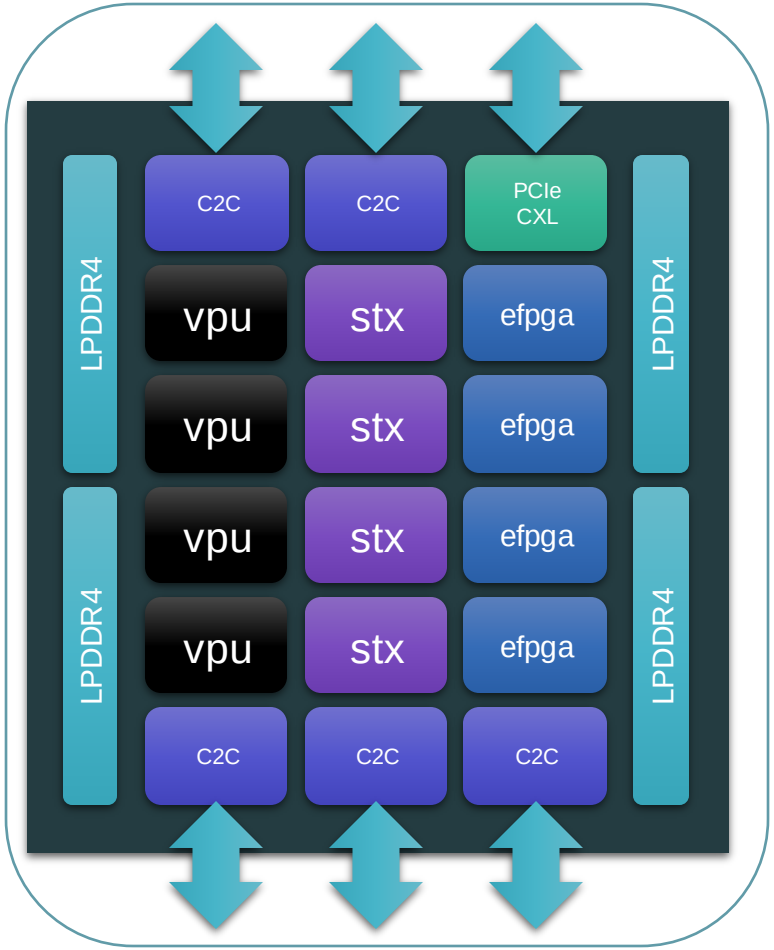
- **Chip**
  - 6 nm and below
  - integrating both CPU and accelerator parts
  - Network on Chip (NoC): mesh linking all components
- **Core**
  - Arm ISA
  - ARM Neoverse V1 core design – 80 cores
  - with 2 SVE256 (Scalable Vector Extension) units
- **Memory hierarchy**
  - Cache subsystem: L1, L2, SLC (System Level Cache)
  - 4 HBM: High Bandwidth Memory
  - 4 DDR5 interfaces (Standard Memory)
- **High speed I/O**
- **Security block – dedicated crypto IP**



Design targets:
- High Byte/Flop ratio
- Compute performance and efficiency for real-applications
- Ideal for HPC & AI inference

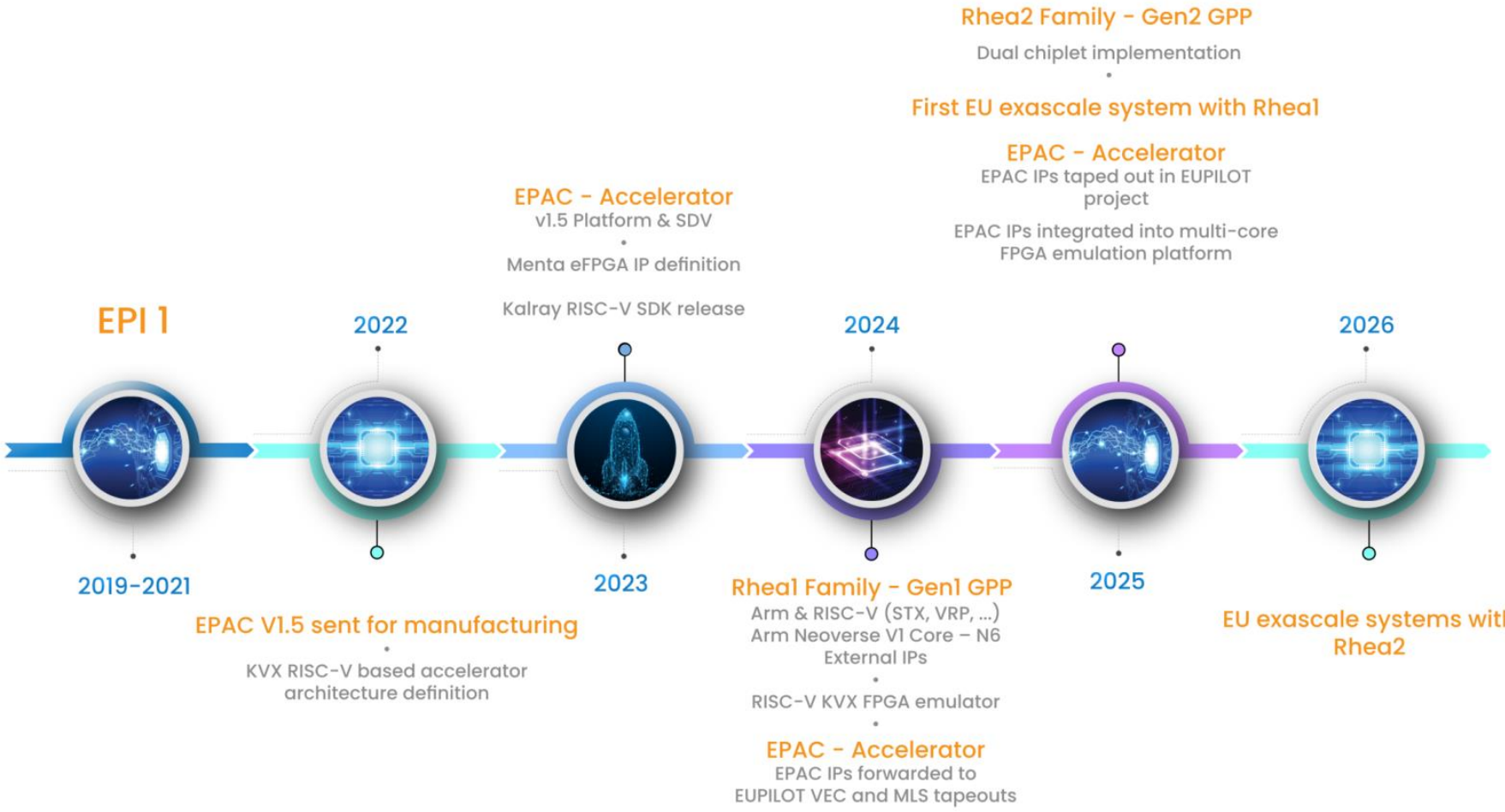
EPAC vision and contributions

- **VEC -** Self-hosted RISC-V CPU + wide VPU (256 double elements) supporting RVV 0.7.1 / 1.0
- **STX -** RISC-V CPU + specific cores for stencil and neural network computation
- **VRP -** RISC-V CPU with support for variable precision arithmetic (data size up to 512 bit)
- **eFPGA -** On-chip reconfigurable logic
- **Ziptillion -** IP compressing/decompressing data to/from the main memory
- **KVX -** FPGA demonstrator of the Kalray RISC-V CPU targeting HPC and ML



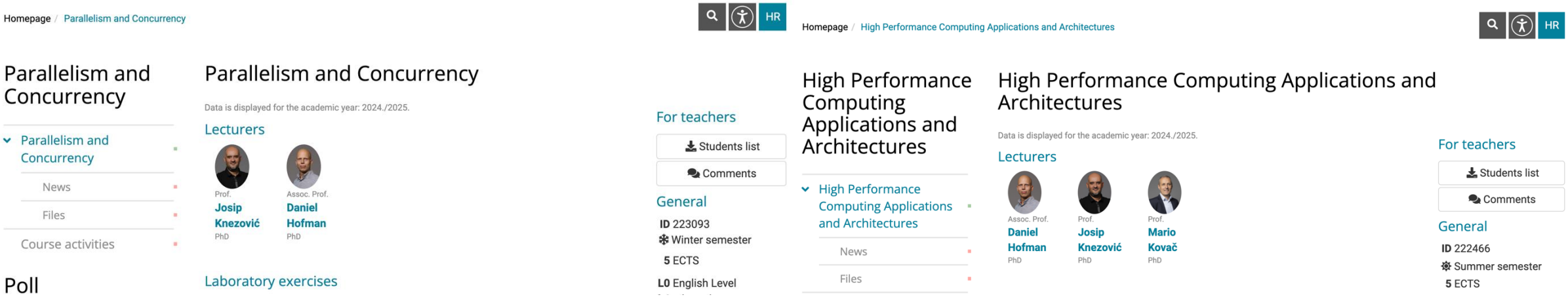
Projects: European Processor Initiative

EPI Timeline:

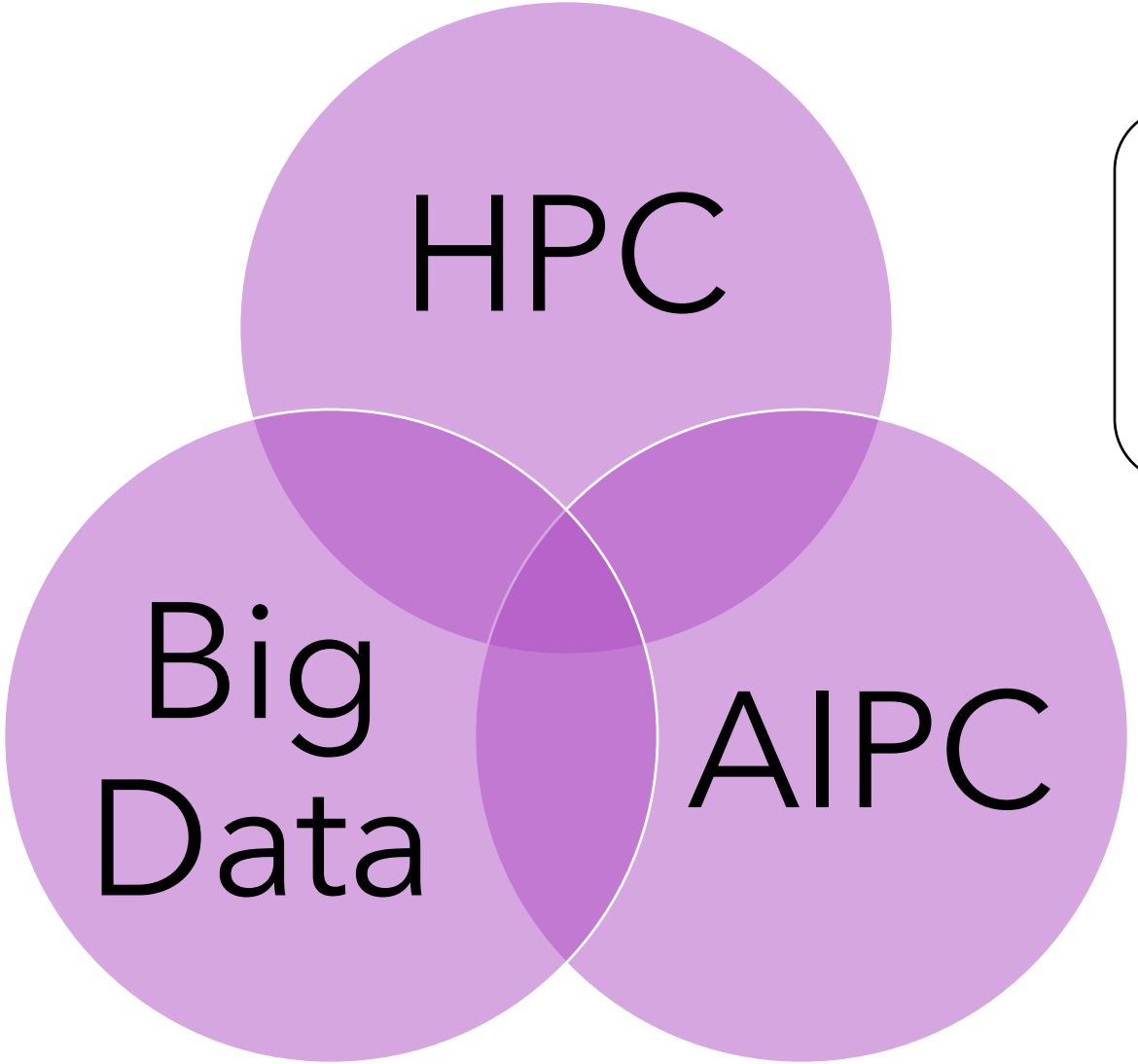


Teaching

- Parallelism and Concurrency
- High Performance Computing Architectures and Applications



Sort of Conclusion



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